

A New Class of Asynchronous Analog-to-Digital Converters Based on Time Quantization

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Concurrent Integrated Systems

Scope of this work

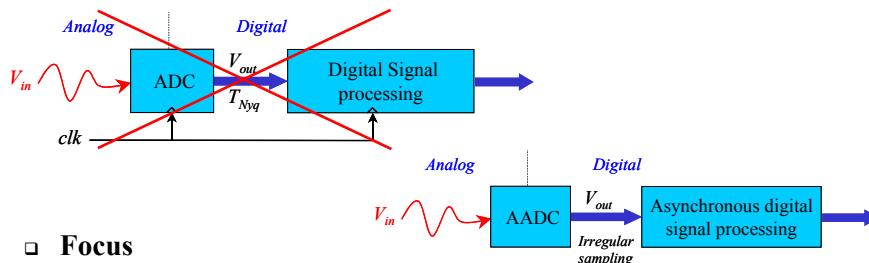
- Context : Integrated Smart Devices & Communicating Objects

➔ Power consumption reduction by more than one order of magnitude

- Solution : Re-think the whole processing chain

➔ The system is only driven by the information of the signal

- Asynchronous design (without any global clock)
- Irregular sampling



- Focus

A/D converter : the **AADC**

Previous works

- **Asynchronous ADCs :**
 - **Kinniment *et al.*** [Kin98]: asynchronous Successive Approximation ADC
 - **Kinniment *et al.*** [Kin99]: micropipelined Flash ADC
 - **Conti *et al.*** [Con99]: asynchronous pipelined ADC
 - **Reduction of power consumption, metastability problems, noise ...**

- **Irregular sampled ADC :**
 - **Sayiner *et al.*** [Say96]: synchronous ADC with irregular sampling
 - **Reduction of activity**

Outline

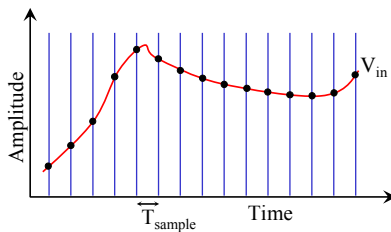
- Irregular sampling vs. regular sampling
- AADC architecture
- General design methodology
- Case study: AADC for speech application
- Results and discussion
- Conclusion and prospects

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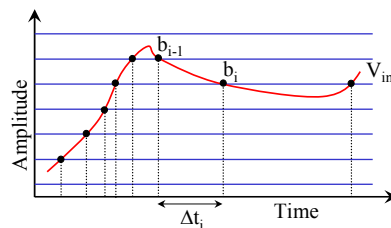
Asynchronous sampling (1)

□ Regular Sampling



- Respect the Shannon theorem
- In an ADC: Amplitude quantization
- Useless samples

□ Irregular sampling [Mar81]



- "level-crossing sampling"
- In an ADC : Time quantization
- No useless sample

Dual
↔

Asynchronous sampling (2) – Summary

	Regular sampling	Irregular sampling
Sample capture	Clock	Level crossing
Amplitude	Quantized	Exact
Time	Exact	Quantized
SNR	Number of bits	Timer resolution
Converter output	V_{out}	V_{out} and Δt

Asynchronous sampling (3) – SNR

□ Nyquist ADC :

- Pure sine wave : $SNR_{dB} = 6,02 \cdot ENOB + 1,76$

□ AADC :

$$SNR_{dB} = 10 \cdot \log \left(\frac{3 \cdot P(V_{in})}{P\left(\frac{dV_{in}}{dt}\right)} \right) + 20 \cdot \log \left(\frac{1}{T_c} \right)$$

➔ Only depends on V_{in} and T_c (Timer period)

– Examples

- Pure sine wave : $SNR_{dB} = -11,19 - 20 \cdot \log(f \cdot T_c)$
- Speech signal : $SNR_{dB} = -66,3 - 20 \cdot \log(T_c)$

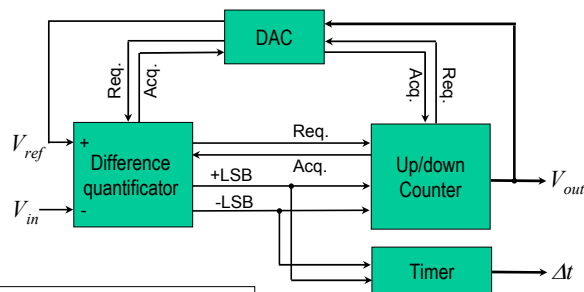
ENOB	T_c^{-1}
8-bit	753-kHz
10-bit	3.01-MHz
12-bit	12.05-MHz
14-bit	48.21-MHz

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AADC (1) – Architecture

- Irregular sampling + Asynchronous design = AADC



If $(V_{in} - V_{ref}) > \frac{1}{2} q$, then : $+LSB = 1$
If $(V_{in} - V_{ref}) < -\frac{1}{2} q$, then : $-LSB = 1$
Else : $+LSB = -LSB = 0$

AADC (2) – Parameters

□ **Quantization :**

- Hardware resolution M
 - Input signal dynamic
- } → Quantum : $q = \frac{\Delta V_{in}}{2^M - 1}$

□ **Timing consideration :**

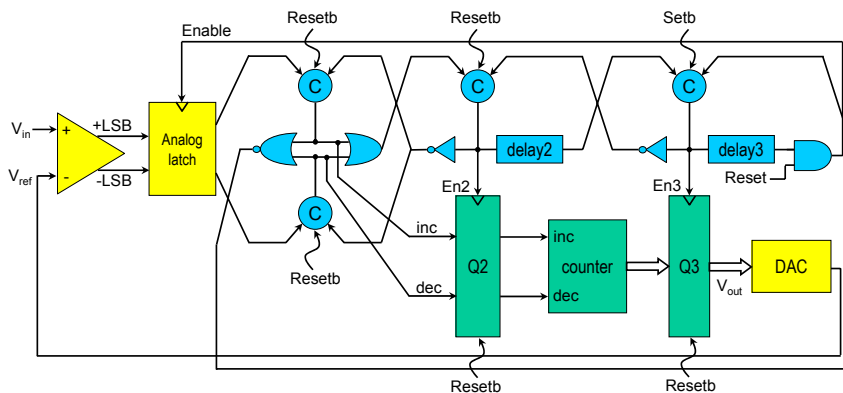
- Finite loop delay δ : V_{in} mustn't cross any quantization level until a conversion is completed

→ Tracking condition : $\left| \frac{dV_{in}}{dt} \right| \leq \frac{q}{\delta}$

AADC (3) – Implementation

□ **Micropipeline Architecture**

- Control part (4-phase)
- Data path part : digital and analog blocks



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Design methodology

- **Purpose :**
 - Minimize activity
 - Power consumption
 - Electromagnetic emissions
 - Minimize complexity
 - Die area
- **Input parameters :**
 - Type of signals to process
 - Power Spectral Density *PSD*
 - Bandwidth f_{max}
 - Input dynamic ΔV_{in}
 - Density probability $p(x)$
 - Targeted application
 - Effective Number of Bits *ENOB*
- **Output parameters :**
 - Maximum loop delay δ_{max}
 - Hardware resolution *M*
 - Timer period T_C
 - Current quantum q_I
(current mode design)
or Unit capacitor C_{unit}
(voltage mode design)

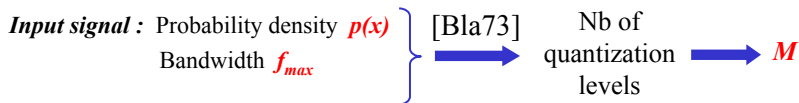
Computing M

□ **Regular sampling :**

Shannon theorem: $f_{sample} \geq 2 \cdot f_{max}$ → Reconstruction is possible

□ **Irregular sampling :** [Beu66]

“Generalized” Shannon theorem $f_{sample} I_{avg} \geq 2 \cdot f_{max}$
 → Reconstruction is possible (theoretically)



Computing δ and q_I (or C_{unit})

□ **Bernstein Theorem:**

A bandlimited f_{max} and amplitude limited ΔV signal V_{in} has a limited slope :

$$\left| \frac{dV_{in}}{dt} \right| \leq 2 \cdot \pi \cdot \Delta V \cdot f_{max}$$

□ **Tracking condition :** if $\Delta V = \Delta V_{in}$:

$$\delta \leq \frac{1}{2 \cdot \pi \cdot (2^M - 1) f_{max}}$$



Computing T_C

Asynchronous ADC : SNR relation

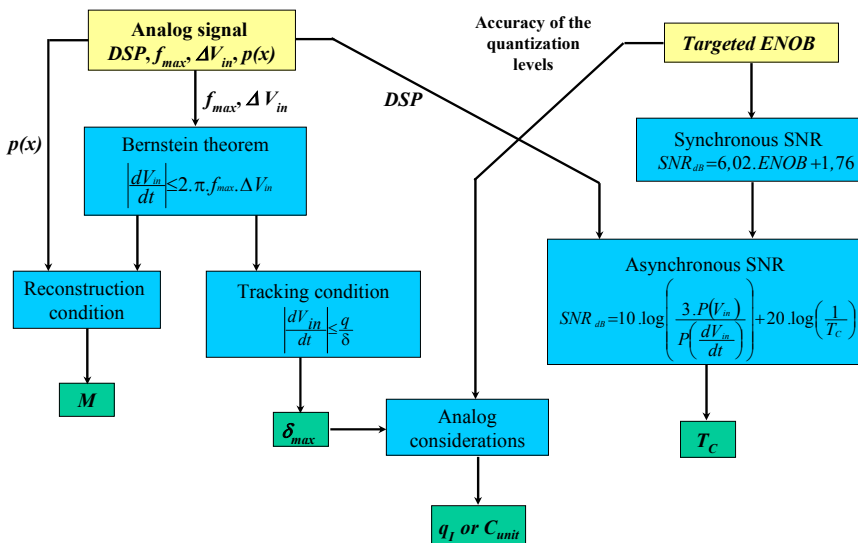
$$SNR_{dB} = 10 \cdot \log \left(\frac{3 \cdot P(V_{in})}{P \left(\frac{dV_{in}}{dt} \right)} \right) + 20 \cdot \log \left(\frac{1}{T_C} \right)$$

Only depends on the application

Only depends on the class on the input signal

T_C is computable

General Flow



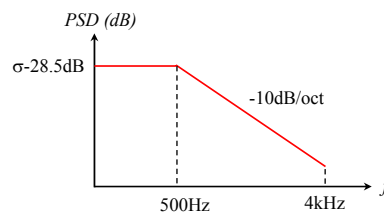
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Input parameters

□ Speech signal :

- Bandwidth : $f_{max} = 4\text{kHz}$
- Power spectral density **PSD**

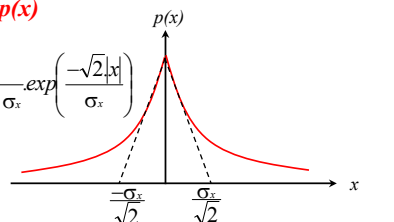


- Input dynamic : $\Delta V_{in} = 5\% \text{ to } 95\% \text{ of } \Delta V_{in}$
- Density probability of the amplitude : $p(x)$

□ Targeted application :

$ENOB \leq 12\text{-bit}$

$$p(x) = \frac{1}{\sqrt{2} \cdot \sigma_x} \cdot \exp\left(\frac{-\sqrt{2}|x|}{\sigma_x}\right)$$



Design parameters computation

- **Reconstruction condition :**

$$M = 4\text{-bit}$$

- **Bernstein theorem & tracking condition :**

$$\delta_{max} = 2.65\mu\text{s}$$

- **Analog considerations : (current mode design)**

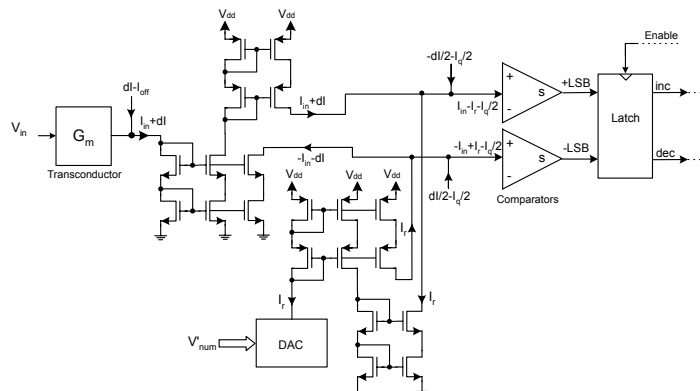
$$q_I = 3.2\mu\text{A}$$

- **Asynchronous SNR :**

T_C^{-1}	ENOB
1.13-MHz	7-bit
2.26-MHz	8-bit
4.52-MHz	9-bit
9.04-MHz	10-bit
18.09-MHz	11-bit
36.19-MHz	12-bit

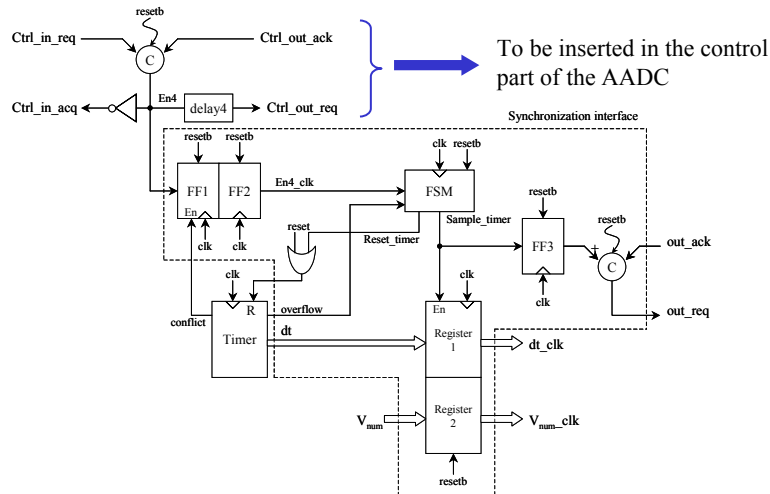
AADC Design : analog part

- **Technology :** CMOS 0.18 μm from STMicroelectronics
- **Analog Design :** current mode



AADC Design : digital part

□ Timer and synchronization interface



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Electrical simulations

Hardware resolution	$M=4\text{-bit}$
Timer	$18\text{-bit}, T_C^{-1} \text{ up to } 36\text{-MHz}$
ENOB	$\text{up to } 12\text{-bit}$
Power supply	$V_{dd}=1,8V$
Input voltage dynamic	$\Delta V=0,8V$
Current quantum	$q_I=3,2\mu A$
Loop delay	$\delta=93ns$
Input signal bandwidth	$f_{max}=114kHz \text{ (Bernstein + tracking)}$
Timer consumption	$P=0,017mW @ ENOB=10\text{-bit}$
Total power consumption when the AADC is inactive	$P_{min}=0,89mW, P_{max}=1,60mW$
Total power consumption when the AADC is active	$P_{avg}=1,71mW \text{ (max. speed)}$
Analog area	$S_{analog}=220\mu m \times 68\mu m$
Digital area	$S_{digit}=160\mu m \times 80\mu m$

Figure of Merit (1)

□ **General Criterion : Figure of Merit :**
$$FoM = \frac{2^{ENOB} \cdot 2 \cdot f_{max}}{P_{avg} \cdot S}$$

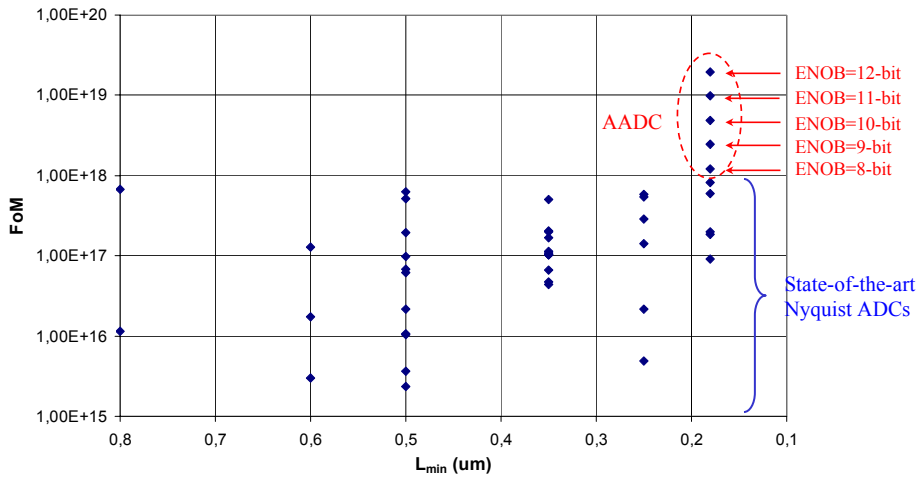
$ENOB [-]$: Effective Number of bits

$f_{max} [Hz]$: Analog input signal bandwidth

$P_{avg} [W]$: Average power consumption

$S [m^2]$: Core area

Figure of Merit (2)



➔ FoM increased by **one order** of magnitude beyond **ENOB=11-bits**



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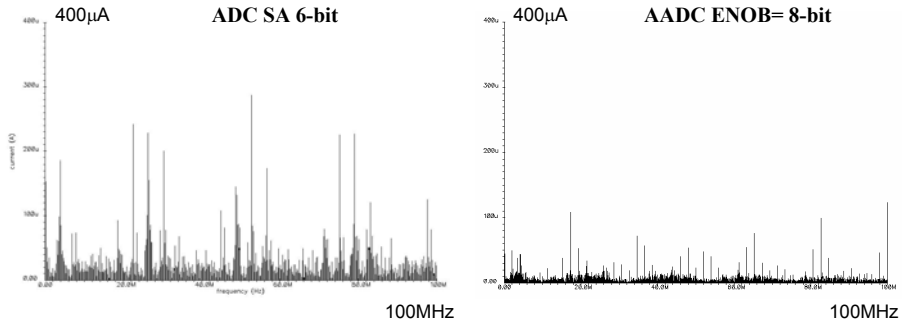
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Electromagnetic emissions

- V_{in} : Full scale input sine wave, $f=90kHz$ (AADC worst case)



➔ Reduction of the maximum current peak by **61,4%** beyond **114kHz**
(pessimistic estimation : no S/H and lower resolution for the ADC)



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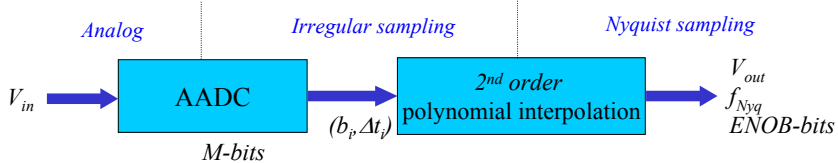
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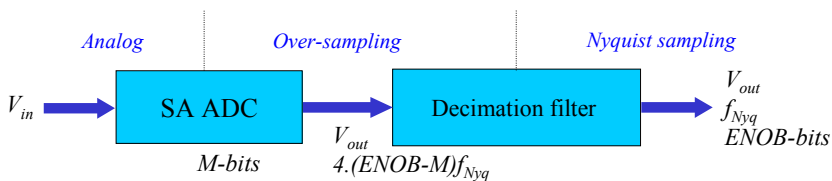
Signal processing considerations (1)

- Purpose : a fully asynchronous SoC but ...
- Possible utilization of the AADC in a Nyquist signal processing environment :
 - AADC output must be re-sampled in a regular way
 - A 2nd order polynomial interpolation preserve the SNR [Say98]



Signal processing considerations (2)

- Synchronous reference : over-sampled Successive Approximation ADC
- 1-bit of ENOB is obtained when f_{sample} is multiplied by 4



Signal processing considerations (3)

- **Decimation and 2nd order interpolation** have the same complexity :

→ Activity \propto Avg Nb of Cycles

<i>ENOB</i>	<i>ADC Nb Cycles/sec</i>	<i>AADC Avg Nb Cycles/sec</i>	<i>Gain</i>
8-bits	512-k	~ 8,2-k	98,4 %
10-bits	768-k	~ 8,2-k	98,9 %
12-bits	1,029-M	~ 8,2-k	99,2 %

→ Activity of the AADC reduced by **2 orders** of magnitude

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Conclusion

- **A new class of ADC** is described :
 - irregular sampling
 - asynchronous design
- A **general design methodology** is also given
- **FoM increased by one order of magnitude** compared to synchronous ADC
- **Activity, power consumption, EMI, area** reduced thanks to :
 - No Sample-and-Hold
 - 1 cycle to convert 1 sample
 - No conversion of useless samples
 - Only *M-bit* hardware resolution is required to achieve *ENOB-bit*

Prospects

- **Architecture optimizations**
 - Another asynchronous implementation
 - Multi-resolution implementation
 - Voltage mode analog design
- **Theory and design of signal processing circuits** on the irregular sampled data stream
- **Fabrication of the prototype**

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