

7.7 Electronic Alignment for Proximity Communication

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Chips placed face-to-face in close proximity can communicate via capacitive coupling if suitable transmit and receive plates overlap as in Fig. 7.7.1. Plates of top-level metal in each chip form the two sides of coupling capacitors used for communication. Capacitively coupled communication is preferable to wired communication for several reasons. First, placing the chips in close proximity completes as many parallel communication paths as are built into the chips without the need for wires. Second, the communication path has low capacitance, so each communication circuit operates at very low power. Third, the capacitive coupling operates through the glass overcoating, obviating static discharge structures. Fourth, the density of communication paths greatly exceeds that available with wired conductive paths such as ball bonds. An experimental chip reported here, built in a 350nm process, places 16 parallel communication circuits on 50 μ m centers.

Unfortunately, communicating between chips through tiny coupling capacitors requires precisely positioned chips, and even with very careful mechanical assembly, the chips still have some residual misalignment of Δx and Δy . Misalignment by half of the receiver plate pitch $P1$ makes each receive plate span two transmit plates, completely destroying the received signal. Satisfactory communication thus requires mechanical alignment in two dimensions such that $|\Delta x| \ll 0.5P1$ and $|\Delta y| \ll 0.5P1$. Such precision is often difficult to achieve and maintain under thermal expansion and mechanical vibration.

To reduce the mechanical alignment needs, an on-chip electronic alignment structure is built. Each transmit plate is divided into 16 "microplates" that together occupy the area opposite a single receive plate. In Fig. 7.7.2, the small squares represent these microplates. The superimposed larger squares represent the receive plates on the other chip. Switching circuits built into the transmit array permit one chip to send its signals to whatever microplates align with the receive plates, thus compensating for mechanical misalignment between the two arrays. In the figure each shaded group of nine microplates shows the ones in use.

The microplates have a pitch $P2$. The test chip has 16 microplates per bit position, making $P2$ one-fourth of $P1$, or 12.5 μ m; however, a different microplate density could be used. Selecting the proper microplates to use for each receiver compensates for misalignment to one-half of the microplate pitch, reducing residual misalignment to at most 6.25 μ m.

Switching circuits that drive data to the proper microplates appear in Fig. 7.7.3. Each microplate can receive data from sources on its left and right. Multiplexer control signals, not shown, choose which data appear on each microplate. This data steering compensates for misalignment in one direction.

To compensate for misalignment in both X and Y directions, the multiplexer circuits must steer data in two dimensions. Figure 7.7.4 shows many microplates and illustrates the steering range for a data bit B2. Nominally, the 4x4 array of cross-hatched microplates surrounding bit B2 transmits its value. However, this 4x4 array can translate anywhere within the 8x8 array of hatched microplates.

The full two-dimensional multiplexer array for one set of 16 microplates appears in Fig. 7.7.5. Four multiplexers above and

four more below the 16 microplates control the horizontal shift. Their output serves as the input to the 16 vertical multiplexers inside the array of microplates. The transmit power for chip-to-chip communication comes from the final set of multiplexers. To save power, microplates whose locations render them ineffective are switched off, as illustrated by the white microplates in Fig. 7.7.2.

The structure of Fig. 7.7.5 compensates for mechanical misalignment up to $\pm 0.5P1$, or $\pm 25\mu$ m. This chip compensates for a greater misalignment because its transmit array is physically larger than its receive array, as shown in Fig. 7.7.7. The transmit array spans 64 receiver plates, in an 8x8 array, but the receiving chip uses only 16 plates, in a 4x4 array. The resulting border of two extra receiver plates around a centered receive array permits chip-to-chip communication even if the mechanical misalignment approaches $\pm 2P1$, or $\pm 100\mu$ m. By appropriately steering data to the microplates, each receive bit is aligned to some transmit bit. This leaves an "integer" misalignment: bits communicate well, but emerge from the receiver on a channel different from nominal.

Compensating for residual integer misalignment requires merely a bit-shifting operation on either chip. In this test chip such bit shifting circuits are simulated in software, which maps receive channels to transmit channels in a manner similar to an on-chip shifting mechanism. Figure 7.7.6 plots results of 3-D field simulations for two chips capacitively communicating over misaligned plates. With misalignment correction, the difference between signal and noise falls to zero only after misalignment exceeds $2P1$, or 100 μ m. Without correction, the useful signal falls to zero within 0.5 $P1$.

Figure 7.7.7 is a partial die photo of the test chip, focusing on the transmit and receive arrays. The 400x400 μ m transmit array consists of 1024 microplates, and the 200x200 μ m receive array consists of 16 plates. Also shown are electronic verniers that measure mechanical alignment to a resolution of about 1.4 μ m [1]. This experimental setup uses standard micrometers to position the two chips. Once the chips are in close proximity, the vernier measurement circuits indicate the remaining error which test software uses to control the steering circuits. Because the misalignment correction is electronic, the multiplexers may be reprogrammed periodically to combat mechanical drift from thermal or vibrational effects.

By sending random bit patterns simultaneously on the 16 channels, data transmission through the steering array is tested. In a 350nm technology the experimental chip communicated at 1.35Gb/s per channel with a BER $< 10^{-10}$.

This work presents a method for reducing the sensitivity of proximity communication to chip misalignment. The experimental chip demonstrates electronic alignment in X and Y to a precision of 6.25 μ m over a range of $\pm 100\mu$ m.

Acknowledgements:

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References:

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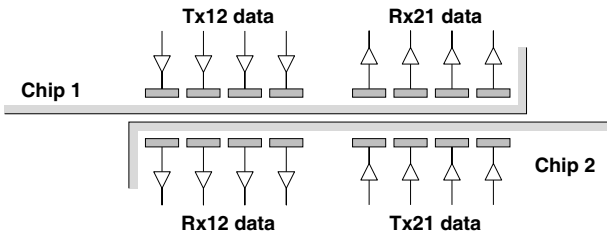


Figure 7.7.1 : Proximity communication cross-section.

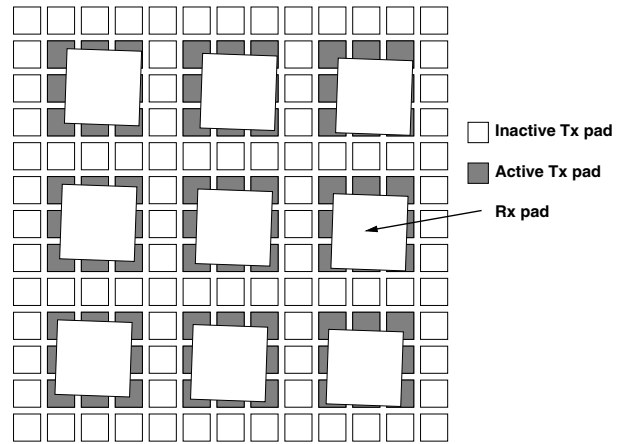


Figure 7.7.2 : Top view of electronic alignment multiplexing.

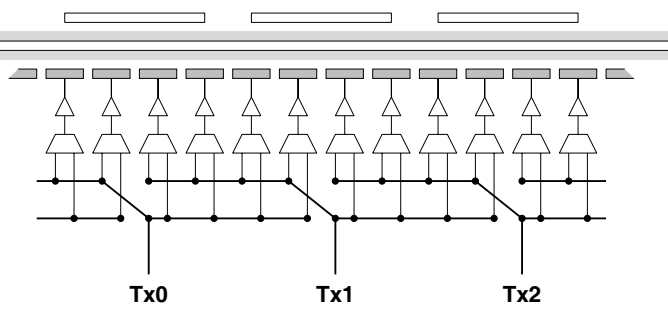


Figure 7.7.3 : Microplate cross-section.

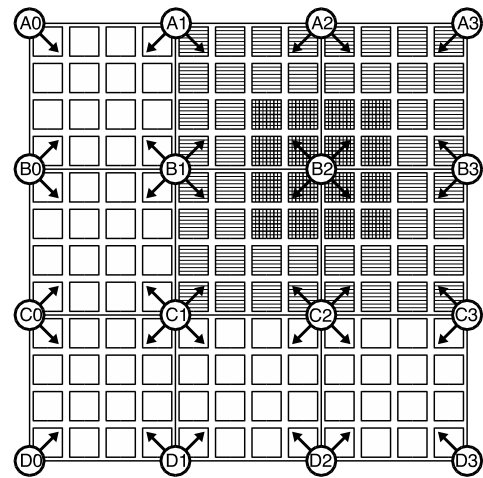


Figure 7.7.4 : Electronic alignment diagram.

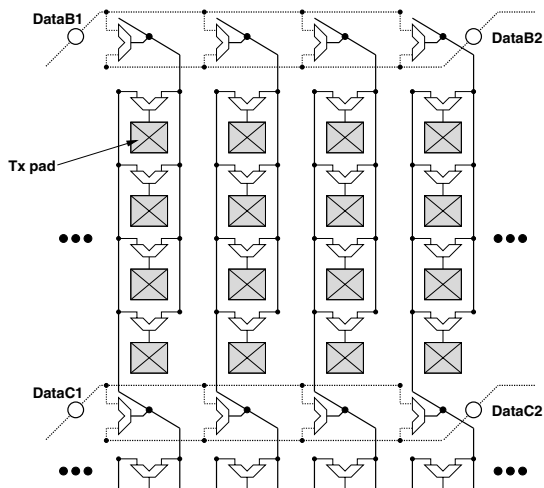


Figure 7.7.5 : Electronic alignment circuit.

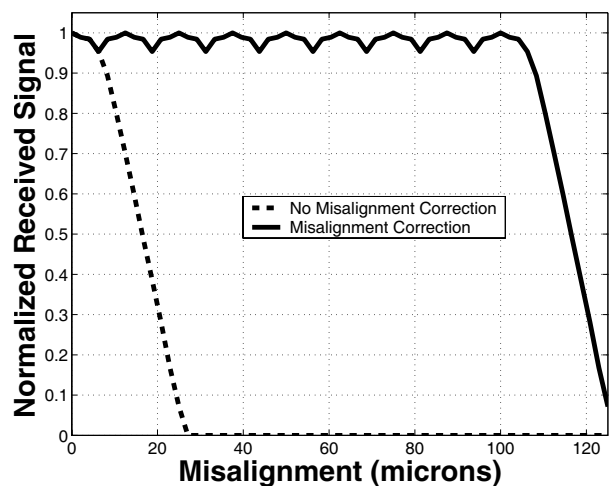


Figure 7.7.6 : Simulated received signal versus X misalignment.

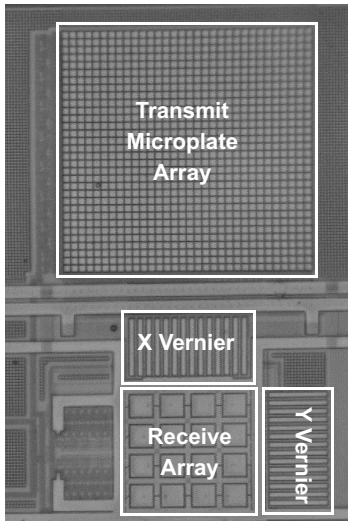


Figure 7.7.7 : Chip photo.

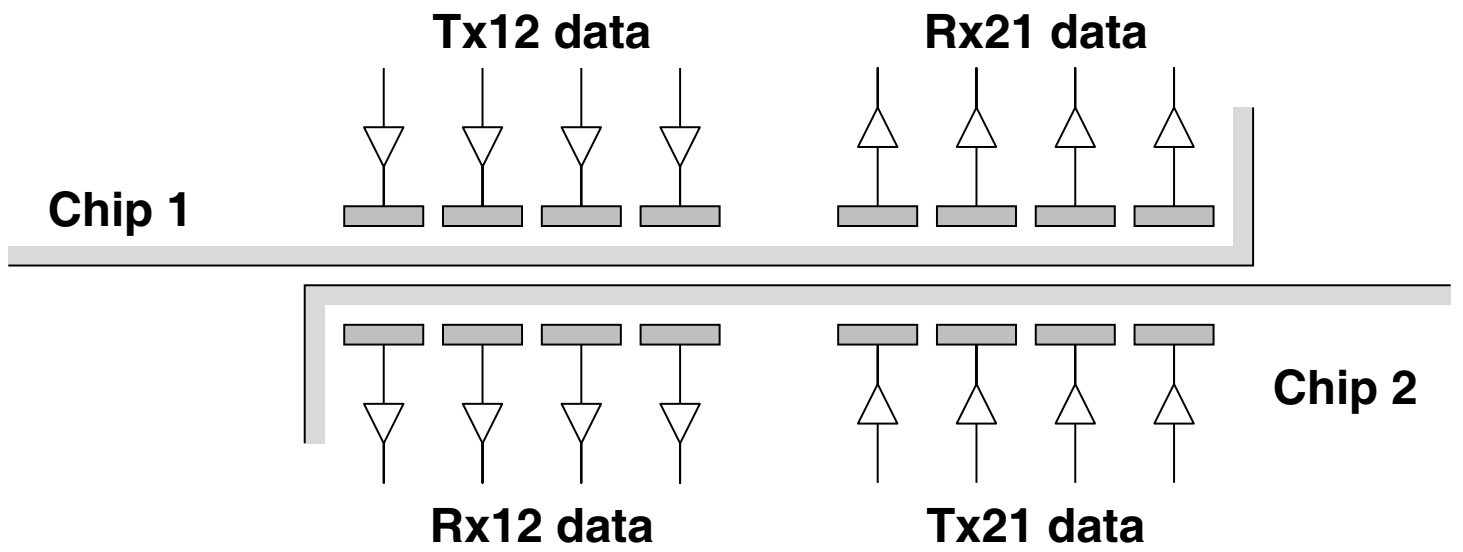


Figure 7.7.1 : Proximity communication cross-section.

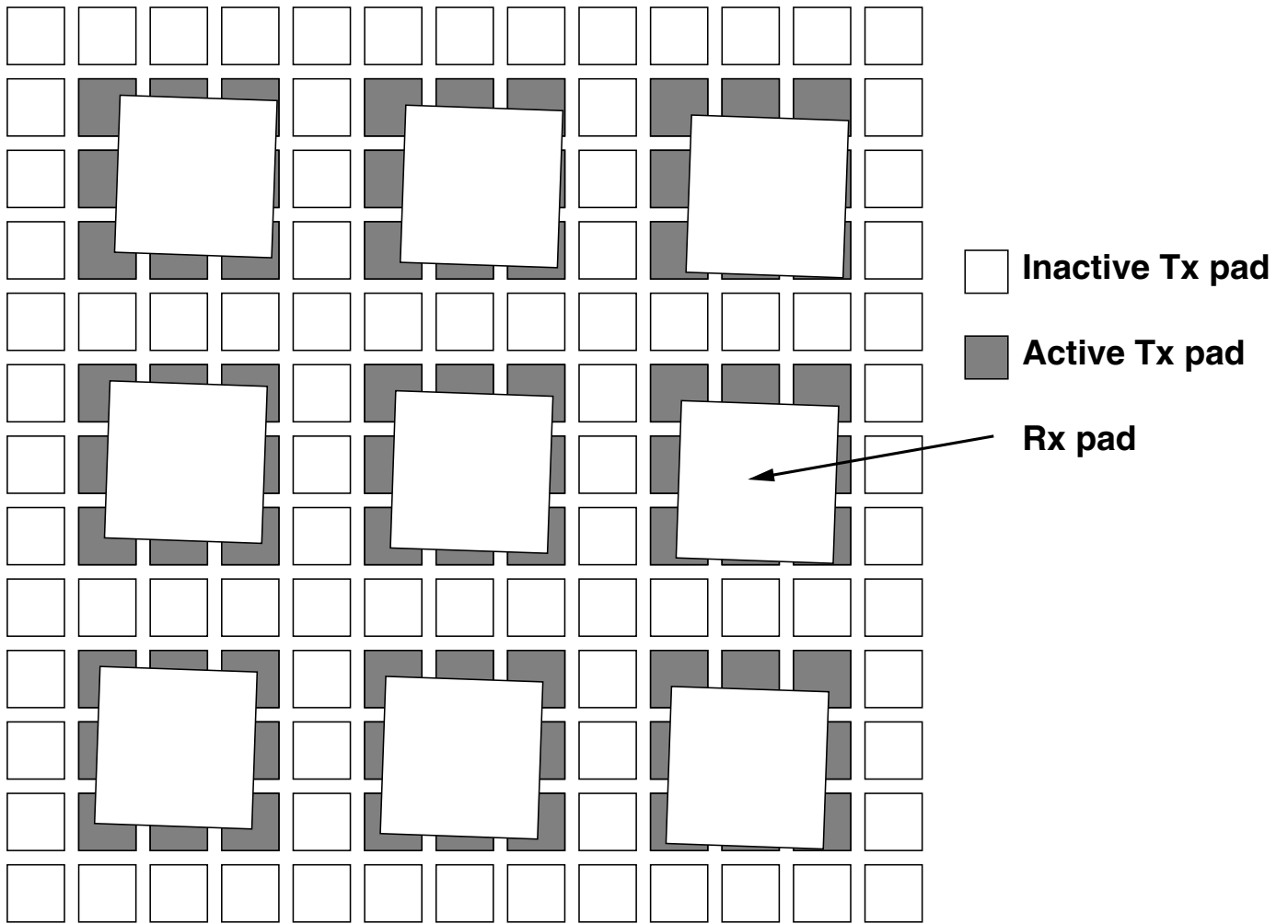


Figure 7.7.2 : Top view of electronic alignment multiplexing.

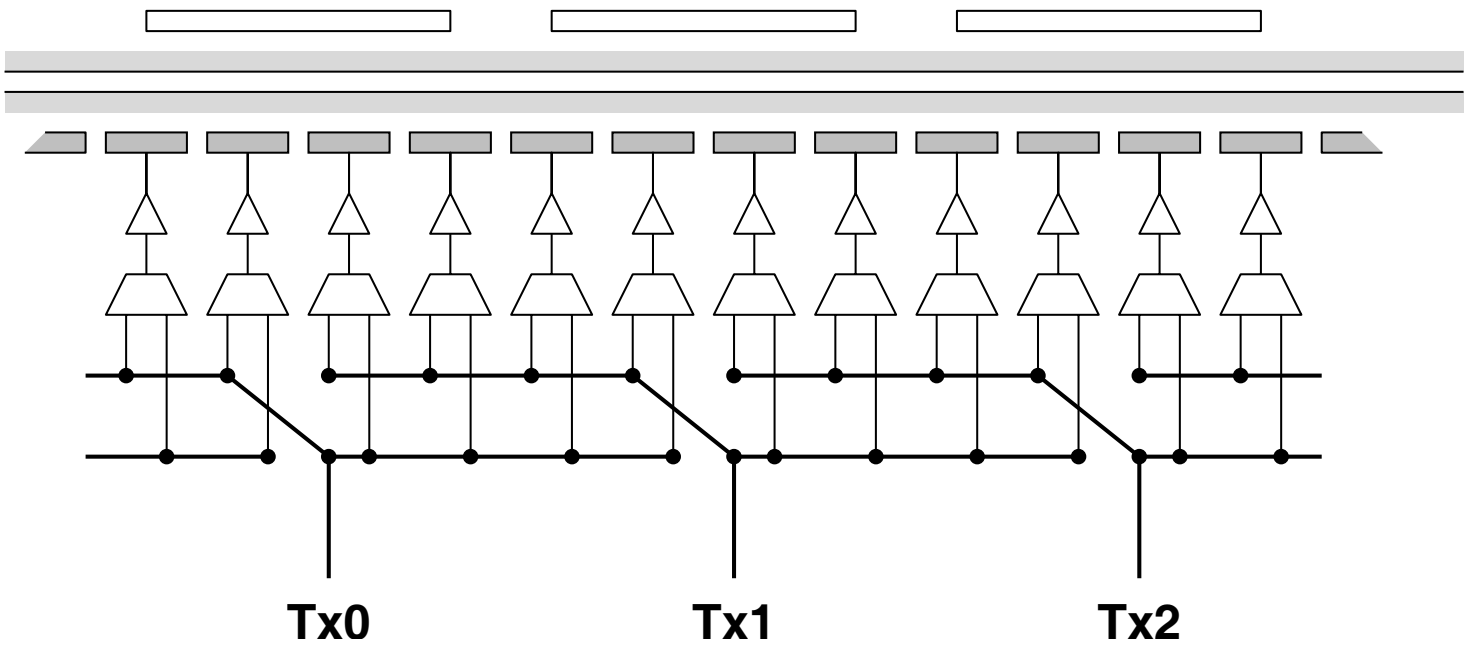


Figure 7.7.3 : Microplate cross-section.

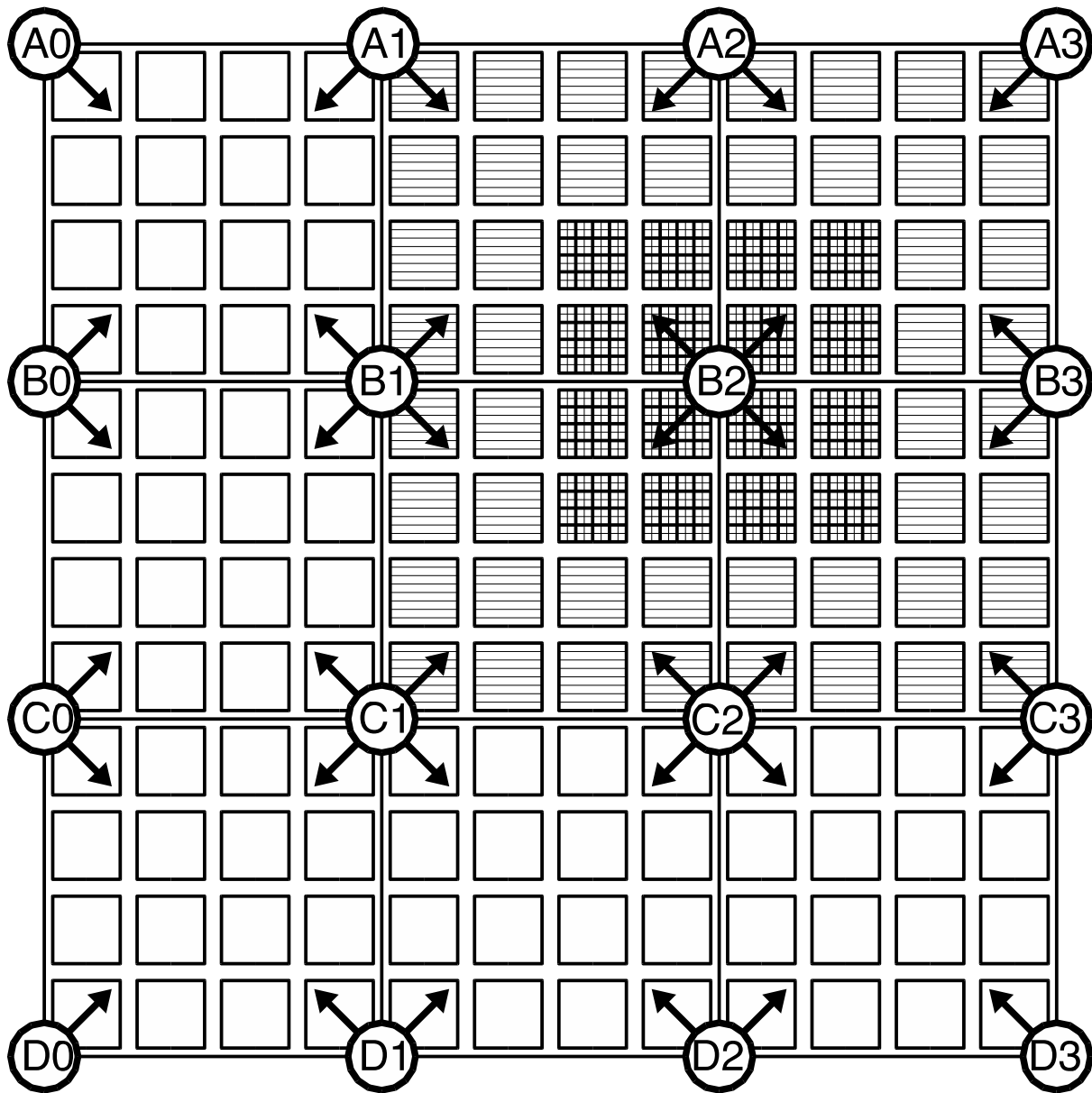


Figure 7.7.4 : Electronic alignment diagram.

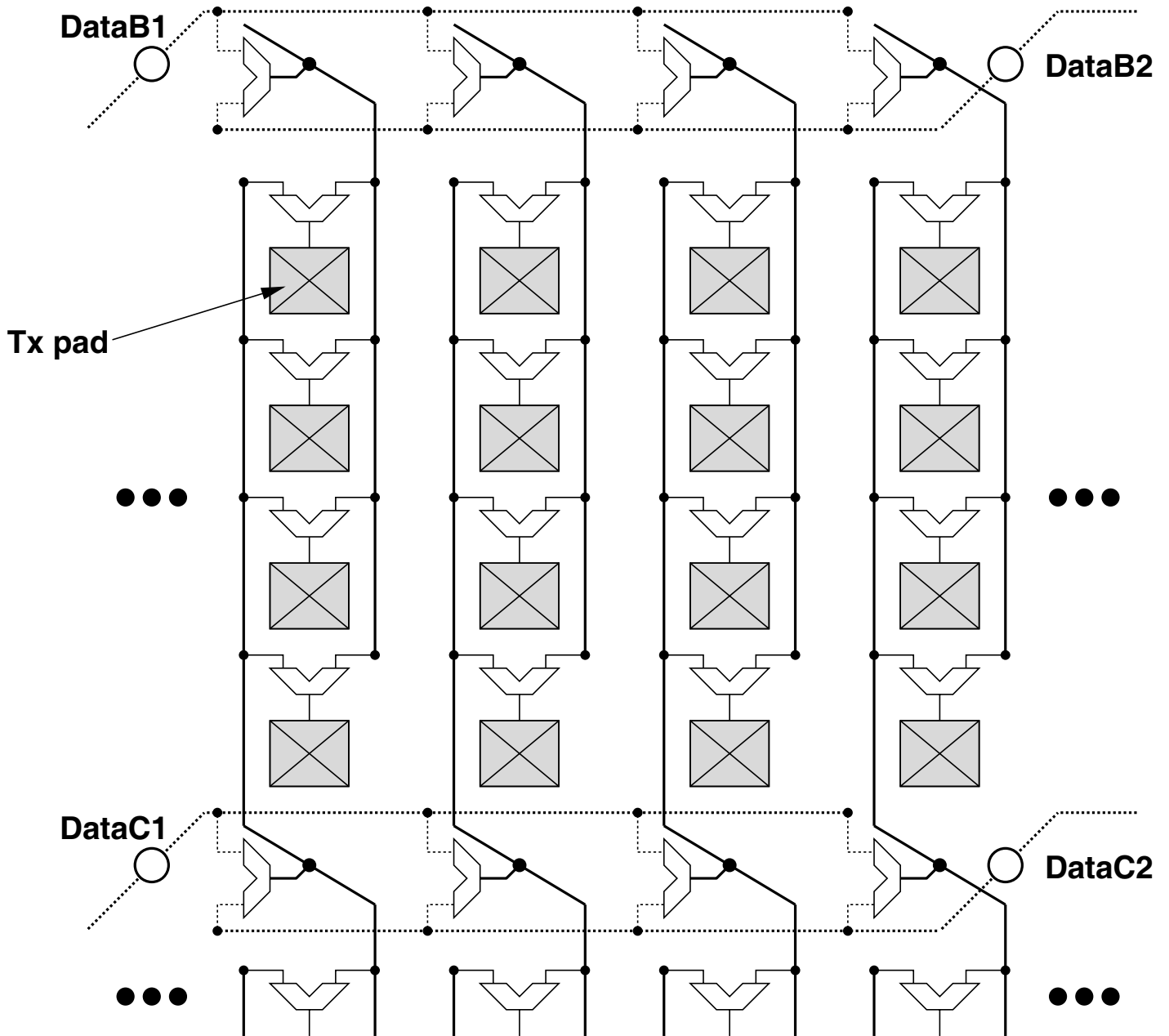


Figure 7.7.5 : Electronic alignment circuit.

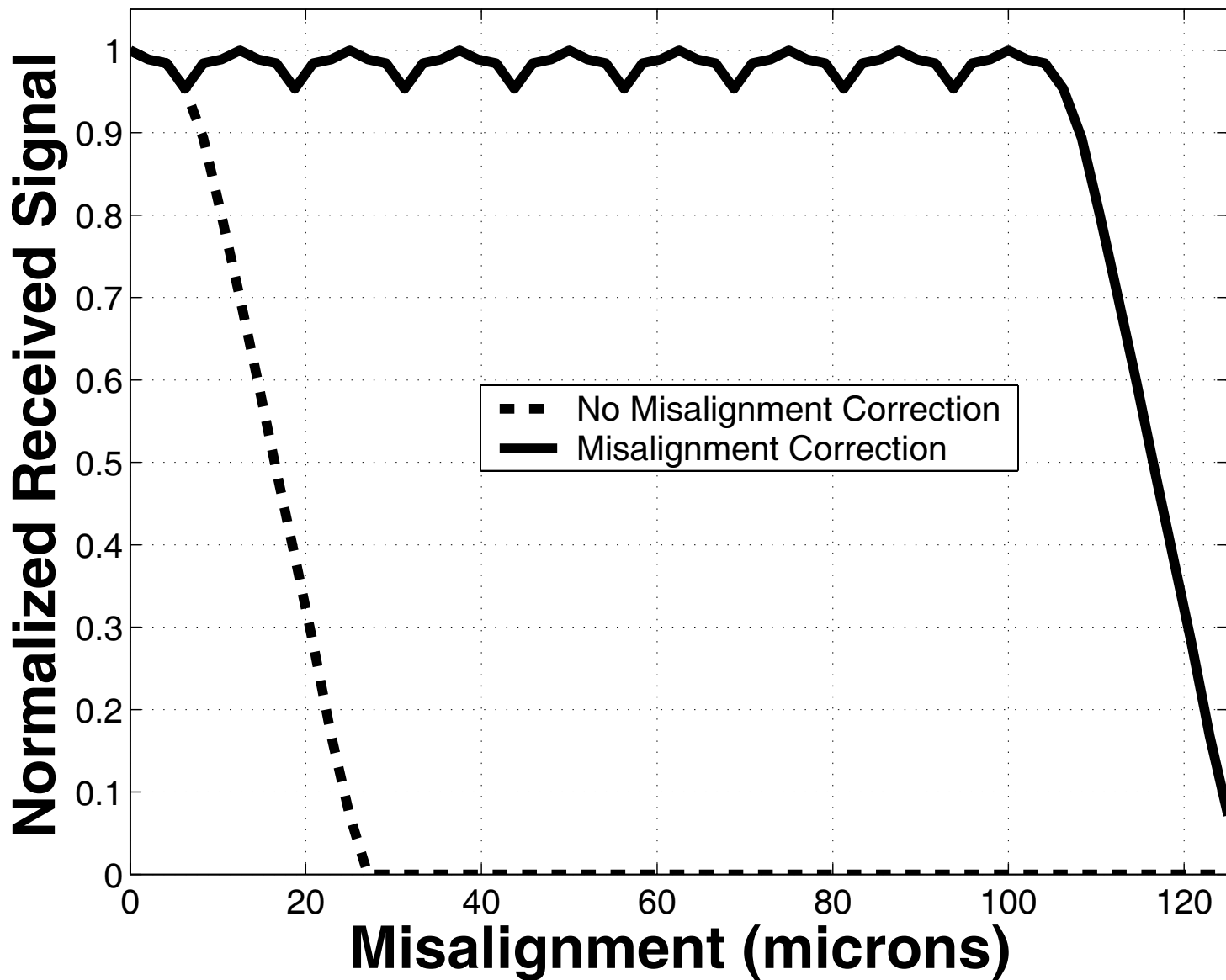


Figure 7.7.6 : Simulated received signal versus X misalignment.

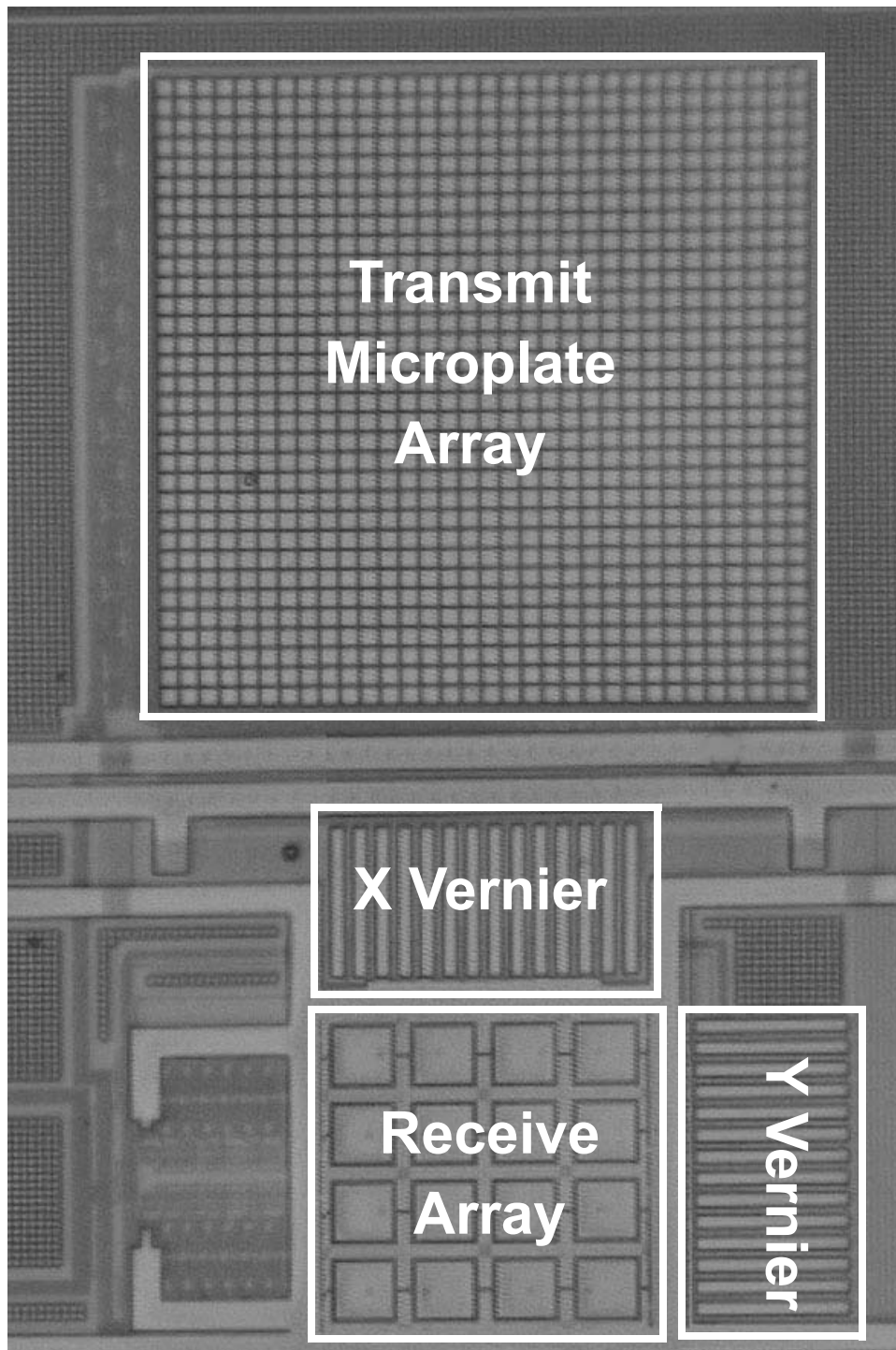


Figure 7.7.7 : Chip photo.