Measuring 6D Chip Alignment in Multi-Chip Packages

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***Abstract*—We present techniques to detect all six degrees of positioning of one CMOS chip relative to another using capacitance measurements. Unlike other capacitive sensing schemes, these solutions achieve sub-femofarad resolution by directly measuring coupling capacitance and rejecting parasitic capacitances. We apply these techniques to dynamically monitor the 6D alignment of chips in multi-chip packages.**

I. INTRODUCTION

CMOS-based sensors that precisely detect position and tilt benefit many mechanical and electronic systems, such as MEMS, robotic devices, instrumentation, and process control. Many existing sensor systems detect position and tilt through mechanical or optical means, making them difficult to integrate into standard CMOS fabrication technologies; in addition, they often detect only a subset of the six degrees of position and tilt.

We present techniques to detect all six degrees of alignment (Fig. 1) between two CMOS chips using measurements of capacitive coupling. The principal challenge to accurately do this is to isolate coupling capacitances from parasitic capacitances. These parasitics include on-chip stray capacitance and capacitive loading from measurement devices, which can dominate the capacitance under test. Existing methods [1,2] infer coupling capacitance by measuring two node capacitances, one with coupling and one without. These methods are sensitive to process variations, especially when the coupling is a small part of the node capacitance.

We show circuits that directly measure coupling capacitances as small as 0.1fF independent of total node capacitance. Using an amplifier feedback technique lets us achieve higher accuracy and resolution than previous approaches [3]. We apply this circuit to dynamically monitor alignment of chips that communicate through Proximity Communication in a multi-chip package.

II. CHIP ALIGNMENT IN MULTI-CHIP PACKAGES

Proximity Communication permits face-to-face chips to communicate through capacitive coupling. This technology eliminates off-chip wires and offers a 100× improvement in bandwidth density [4]. It enables non-soldered connections between chips, improving yield through individual chip replaceability in multi-chip packages. However, it requires precisely positioned chips so that signals are well-coupled between transmitting and receiving channels. Accurate measurements of chip positions let us compensate and correct for any mechanical misalignment through electronic alignment correction [5].

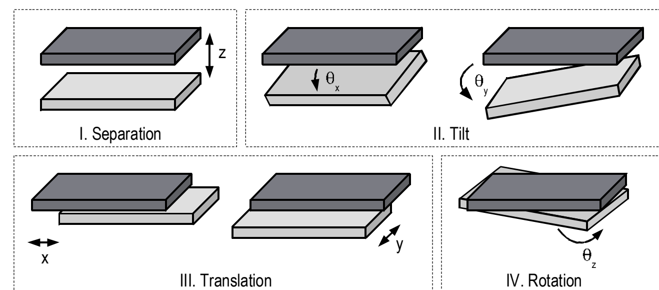

Figure 1. Six degrees of spatial alignment

We determine chip alignment in all six independent degrees (Fig. 1) by measuring the coupling capacitance between top-level metal plates on two chips [6]. We determine chip separation (z) by comparing the measured capacitance to detailed 3D field solver simulations of a chip-to-chip plate model. Tilt angles (θ_x, θ_y) are determined by measuring z at different locations on the chips.

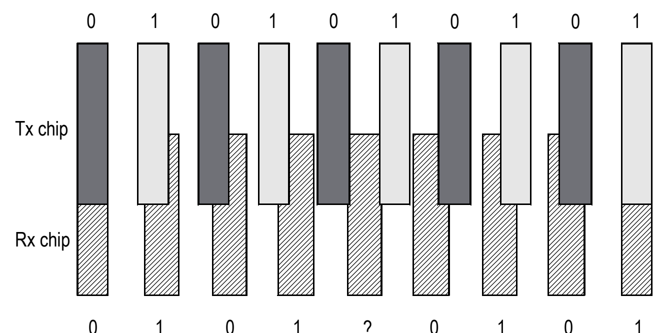

Figure 2. Measuring in-plane alignment using Vernier bars

To measure in-plane alignment (x, y), we use a Vernier technique and measure patterns of capacitance coupling

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beats between rows of plates separated by slightly different pitches on the two chips, as shown in Fig. 2 [4]. This technique provides resolution that is equal to the difference in plate pitch; it is thus limited only by linewidth, and can be very precise.

To accurately measure the angle of in-plane rotation (θ_z), we can exploit the moiré effect, which effectively amplifies small rotation angles into very large spatial periods (Fig. 3) [7]. For plates separated by a pitch of p_t on the transmitting chip and p_r on the receiving chip, the angle of rotation θ_z can be found from the spatial interference period λ as

$$\theta_z = \cos^{-1}\left[\frac{1}{2}\left(\frac{p_r}{p_t} + \frac{p_t}{p_r} - \frac{p_r p_t}{\lambda^2}\right)\right]. \qquad (1)$$

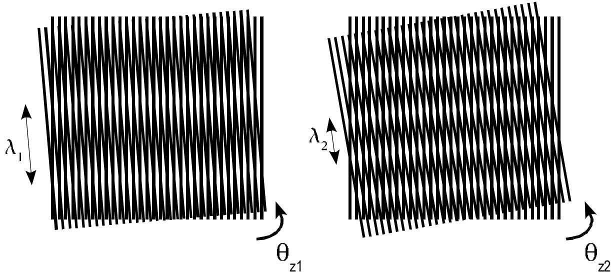

Figure 3. Measuring in-plane rotation using the moiré effect

III. CAPACITANCE MEASUREMENT CIRCUITS

A. Basic Rectifier

Fig. 4 shows a circuit [8] that measures the capacitance C_c in the presence of parasitic capacitances C_1 and C_2. A clock with a voltage swing of V_s applied to node *A* transfers charge $C_c{\cdot}V_s$ on rising edges, and a return charge $-C_c{\cdot}V_s$ on falling edges. A rectifier after node *B*, controlled by $r_p(t)$ and $r_n(t)$, steers all positive charge through switch S_P and all negative charge through S_N. A current meter with input capacitance C_{load} measures the average current through S_P. For a clock frequency of f_s, the average measured current is

$$i_{avg} = C_c\, V_S\, f_s\,. \qquad (2)$$

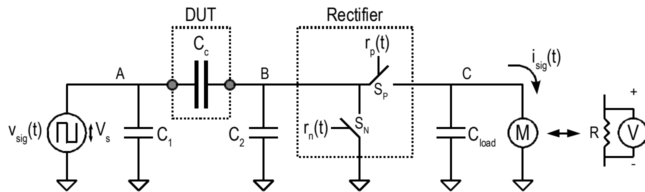

Figure 4. Rectifier circuit that measures capacitance C_c

For correct operation, the signals $v_{sig}(t)$, $r_p(t)$, and $r_n(t)$ obey the phase relationships shown in Fig. 5, where a HI level of $r_p(t)$ and $r_n(t)$ turns on the corresponding switch, and a LO level turns off the switch.

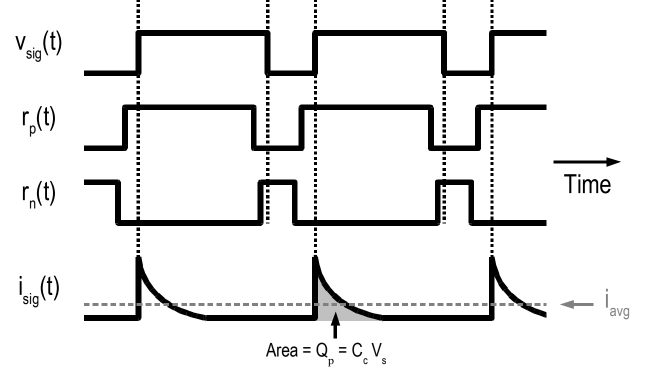

Figure 5. Phase relationships between signals $v_{sig}(t)$, $r_p(t)$, and $r_n(t)$

Because the meter provides the only path to ground after switch S_P, it measures all charge coupled through C_c from rising clock edges, regardless of parasitic capacitances C_2 and C_{load}, even if they are much larger than C_c. A higher clock frequency increases the average current and improves sensitivity and signal-to-noise ratio; however, f_s is limited by the maximum rate at which charge drains into the meter. The coupled signal discharge path has a time constant of

$$\tau \cong (C_c + C_2)(R_p + R) + C_{load} R \qquad (3)$$

where R_p is the resistance through S_P. Switch S_P must conduct for a period much longer than τ so that all coupled charge is drained and measured before S_N conducts. Otherwise, a fraction of the coupled charge drains to ground, and the measured current no longer indicates C_c. Leakage current similarly shunts current away from the current meter, introducing error.

B. Feedback Rectifier

To improve sensitivity, we add a feedback path [9] (Fig. 6) to relax the requirement that the transferred charge be completely drained through the current meter within each cycle. Instead of connecting the rectifier shunt (node *D*) to ground, we drive the rectifier output back to the rectifier shunt, using a unity-gain op-amp. Now, the transferred charge need not completely drain through the meter each cycle. Any residual voltage is fed back to the next cycle through node *D*, increasing the output voltage each cycle until it reaches steady-state DC, when the average current coupled through C_c equals that flowing through the meter.

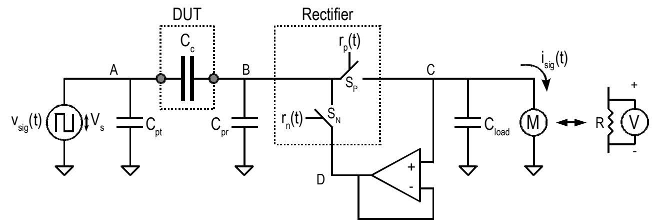

Figure 6. Feedback rectifier circuit for improved measurement sensitivity

Now, the timing requirement between $r_p(t)$ and $r_n(t)$ is that the voltages across the switches equalize during the time

that they conduct. This is dominated by the time constant through S_P,

$$\tau_P \cong R_P \left(\frac{1}{C_2 + C_c} + \frac{1}{C_{load}} \right)^{-1}. \qquad (4)$$

Because the switch resistance R_P is much lower than the resistance R of the current meter, and on-chip parasitics are much lower than loading from the meter, $R_P \ll R$ and $C_2 + C_c \ll C_{load}$. Therefore, $\tau_P \ll \tau$, making measurement frequency and sensitivity much higher. This also reduces the effect of leakage current.

IV. EXPERIMENTAL RESULTS

We built a test chip in 0.18µm CMOS to measure the spatial alignment between two chips, using the techniques mentioned above. We placed two chips face-to-face (Fig. 7), one fixed and one resting on a 6D micro-positioning system [10] that can translate in steps of 0.1µm and rotate in steps of 2µrad.

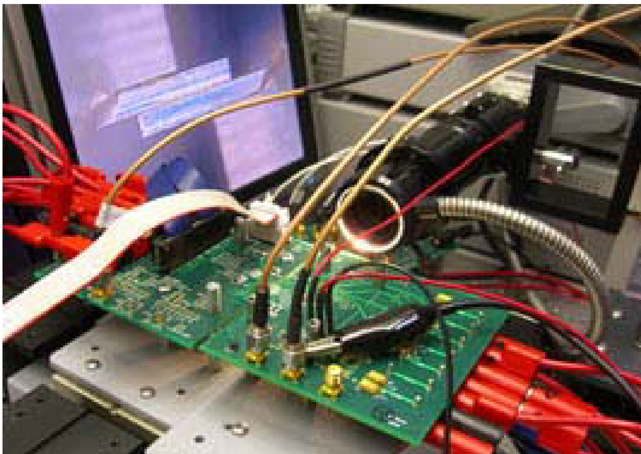

Figure 7. Experimental test setup

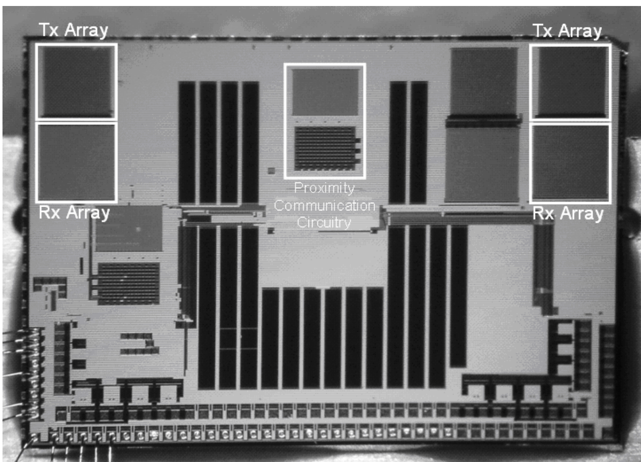

Figure 8. Die photo

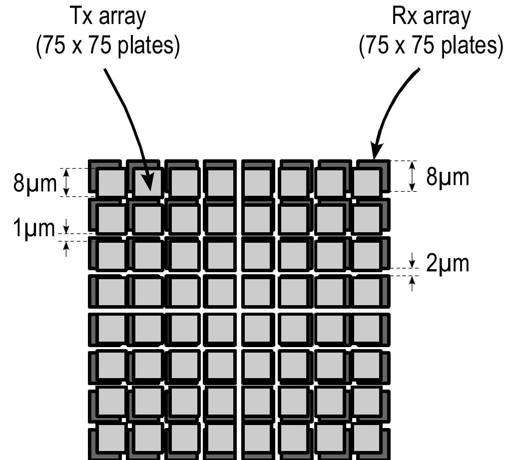

Figure 9. Reconfigurable array of metal plates

Both chips had a planar array of 75 × 75 metal plates (Fig. 8). A subset of plates can be activated and others deactivated, allowing us to test different plate sizes and shapes with the same reconfigurable structure. All plates are 8µm wide, placed on a 9µm pitch on the transmitting chip, and 10µm on the receiving chip (Fig. 9). The difference in pitch allows us to use the Vernier effect to measure in-plane alignment (x, y).

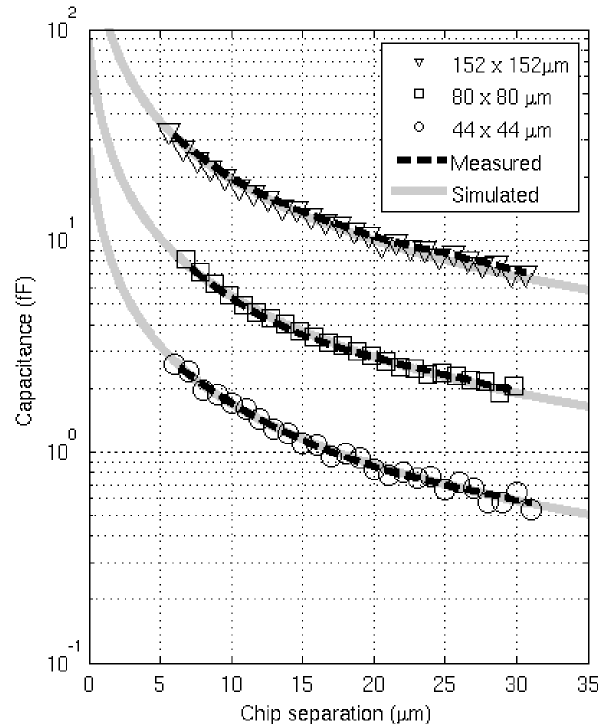

Figure 10. Coupling capacitance vs. chip separation (z)

We used the amplifier feedback circuit of Fig. 6. All circuitry is built on-chip except the feedback buffer [11]. An Agilent 34420A voltmeter in parallel with a 100kΩ resistor

measured the rectified current. For all measurements, the signals had a voltage swing of 1.8V and a frequency of 100kHz.

Fig. 10 shows measured coupling capacitance as a function of chip separation z for three plate sizes, with results from 3D field solver simulations [12] of the same structures. The quoted chip separation is the distance between chip surfaces, and does not include the oxide thickness above the top-level metal. The difference between measured and simulated capacitances was under 40aF, or 4%. From these capacitance measurements, we can determine chip separation with a resolution of 0.2μm.

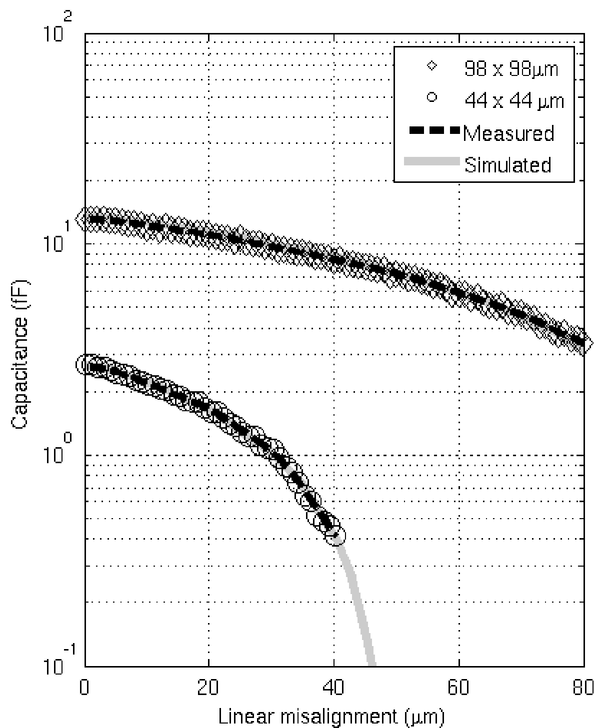

Figure 11. Coupling capacitance vs. in-plane translation (x, y)

Fig. 11 shows measured coupling capacitance as a function of in-plane translation in one direction, for two plate sizes at a chip separation of 6.5μm. From these measurements, we achieve a resolution equal to the difference in plate pitch of 1μm. Results are consistent with simulations, differing by under 30aF or 3%.

V. SUMMARY

We presented a position and tilt sensor that precisely determines all six degrees of alignment. It can be fabricated using a traditional CMOS process, and thus can be readily integrated into electronic devices for in-situ position monitoring of chips in multi-chip packages. The sensor determines alignment through capacitance measurements; this capacitive sensing scheme achieves sub-femtofarad resolution, and is different from most other techniques because it directly measures coupling capacitance and rejects all parasitic capacitances. While our test chip demonstrates the use of this sensor for Proximity Communication, the circuit finds applications in other mechanical and electronic systems, such as MEMS, robotic devices, and electronic instrumentation.

ACKNOWLEDGMENT

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