

## Optical Proximity Communication in packaged SiPhotonics

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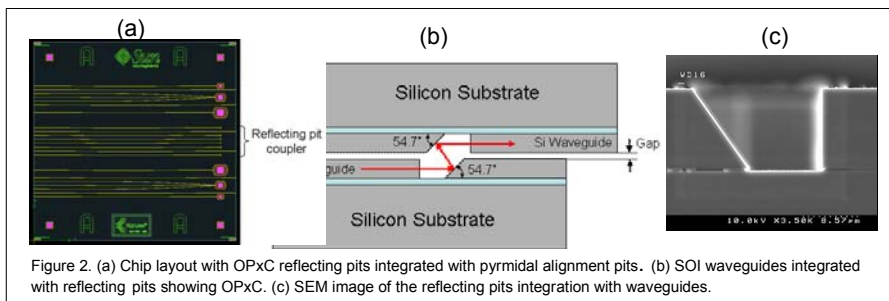
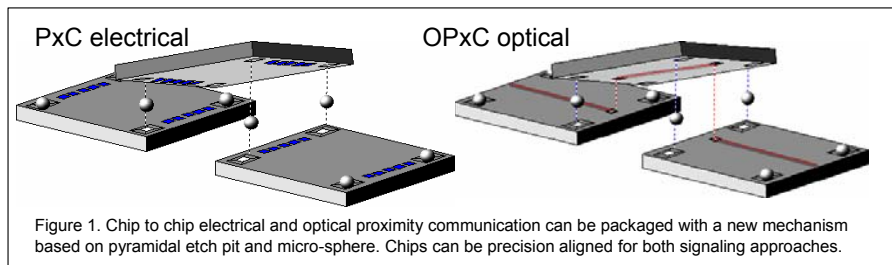
**Abstract:** We report 10Gb/s Optical-Proximity-Communication with reflecting mirrors micro-machined into Si and co-integrated to low loss SOI waveguides for chip to chip communication using a self-aligned-packaging mechanism with measured 4.0 dB coupling loss.

There continues to be growing interest in scaling high performance computing to meet the ever-increasing computational demands generated by new applications from military and commercial sectors. To date architects are combating these challenges by devising processor chips with multi-core, multithreaded solutions as well as attempting higher speed clocking. But demand from high-end applications continues to grow at an even greater pace. Processors with up to 8 cores and 64 threads are now commercially available [1] and an 80-core experimental processor has been proposed [2]. New system topologies containing multiple chips, each with multiple-cores and multi-threading would represent a major advancement if the inter-chip network and routing topologies can achieve the required capacity, functionality and latency. It is challenging to scale the required off chip communication bandwidth by traditional electrical signaling methods such

as Serdes where projections predict significant processor real estate and power to be consumed. On the other hand electrical Proximity communication, PxC, using capacitive coupling

can alleviate part of the bottleneck [3]. As shown in Figure 1, capacitive coupling between micropads on chips can be used to achieve low power, high bandwidth density communication without having to escape the package as is typically the case in traditional electrical signaling. Aggregate bandwidth density of fifty gigabits/cm<sup>2</sup>, and power efficiency of 3.6pJ/bit has been reported for PxC [4]. Still from a latency perspective, electrical paths across on-chip geometries when based on PxC combined with on chip wiring is typically limited to velocities less 1/10 the speed of light.

Optical signaling based on Silicon photonics, on the other hand, could potentially alleviate the off-chip bandwidth bottleneck as well as provide low latency communication. SOI waveguides can transport



signals with greater density and faster than on-chip wires. In addition, with WDM, a single Silicon waveguide can potentially carry many 20Gbps wavelength channels achieving much higher density over on chip wires and potentially reach bandwidth densities of ten petabits/cm<sup>2</sup>. There remains however the distinct challenge of maintaining high fidelity signaling across a multi-chip geometry with low loss coupling and broadband transmission in order to seamlessly build routing networks for advanced system architectures. Here we report a new technological advancement of 10Gb/s Optical Proximity Communication (OPxC) with reflecting mirrors micro-machined into Si and co-integrated to low loss SOI waveguides for chip to chip communication using a self-aligned-packaging mechanism with measured 4.0dB coupling loss. High fidelity optical signaling in a package is demonstrated. To date neither type of PxC signaling in Figure 1 has been reported in a package.

Figure 2 shows fabrication of OPxC which is based on Si micro-machining SOI features with an anisotropic wet etch to create (111) facets that form inter-planar angle of 54.7 degrees with the (100) surface of the chip. Co-fabricated simultaneously with the couplers are the pyramidal pits used for the ball and pit alignment mechanism. The reflecting facets are etched after building 10 micron wide ridge waveguides on an SOI wafer consisting of a 12 micron thick Si layer above a 0.4 box followed by Al metal coating the sidewall of the reflecting pit. An antireflection dielectric coating was deployed to minimize back reflections in the waveguides. The appropriate coatings were only applied to the reflecting sidewall and to the ridge waveguide facet. Figure 2c shows an SEM of the integrated reflecting pit and waveguide. Figure 2a shows the chip layout containing alignment pits designed for a zero chip-gap as depicted in Figure 1 that was geometrically solved with a 400 micron diameter sapphire ball. The precision alignment properties of the ball and pyramidal pit for controlling the six degrees of chip misalignment are discussed in extensive detail in ref [5]. A brief summation is as follows. Our alignment mechanism eliminates five degrees of chip misalignment (to lithographically defined tolerances below 1 micron ) and controls the sixth degree of freedom , the chip gap, to submicron accuracies defined by the precision of the ball dimensions.. The tunability of the gap is a key innovation in this packaging approach that ultimately can lead to chip rematability thereby enabling large arrays of chips to be packaged. Nevertheless, one important aspect of controlling the chip gap (z -separation) is clarified in Figure 2(b) that shows geometric transport of light in the face-up waveguide when coupled into the face-down waveguide. Si micromachining typically produces an angle of 54.7 degrees as opposed to the more ideal case of a 45 degrees reflector. In the latter the exact position of the pit relative to the ball and alignment pit creates coupling conditions that are independent of z where as for the 54.7 reflector the beam walks off the pit for different chip gaps. The two angular cases are shown in Figure 3(a) and hence a 45 degree reflector is more tolerant to the z gap . Figure 3 (b)

gives calculated and measured excess loss for a 54.7 degree reflector as a function of chip lateral misalignment that was reported for a two chip assembly taken with a six axis nanopositioning stage in ref [6]. The measured coupling loss for the three chip package was 0.5 dB more loss per OPxC hop over that achieved with a six axis

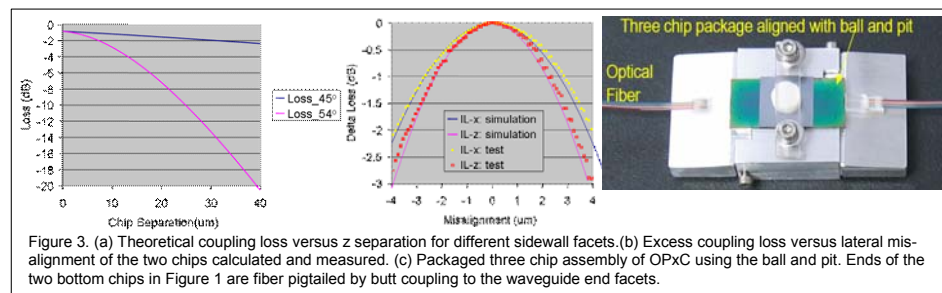
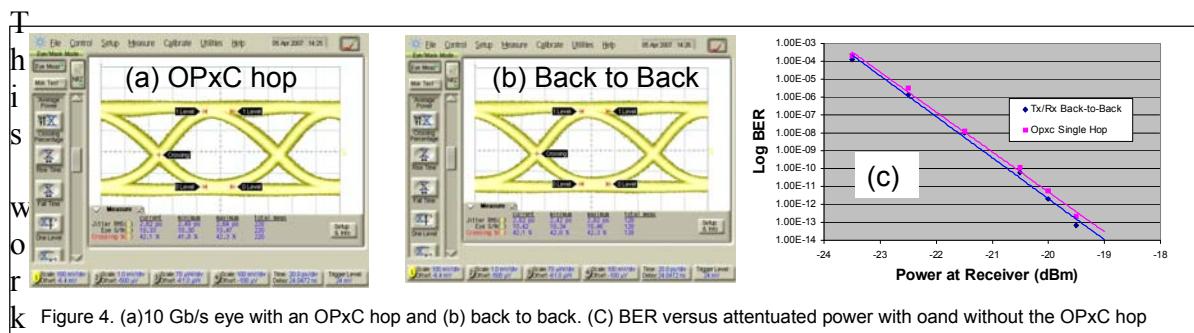


Figure 3. (a) Theoretical coupling loss versus z separation for different sidewall facets.(b) Excess coupling loss versus lateral misalignment of the two chips calculated and measured. (c) Packaged three chip assembly of OPxC using the ball and pit. Ends of the two bottom chips in Figure 1 are fiber pigtailed by butt coupling to the waveguide end facets.

nanopositioning stage suggesting that the package could align chips to within fractions of a micron misalignment.

OPxC maintains high fidelity signaling as measured by BER at 10Gbps and shown in Figure 4. The back-to-back and OPxC eye are virtually indistinguishable as can be visually confirmed. Indeed the rms jitter, deterministic jitter and Q, the Signal to Noise metrics, differ by less than 0.5% when an OPxC hop is inserted into the link. Likewise the sensitivity curves obtained under attenuation are identical and further support the eye characteristics. This is an important conclusion since for the first time the ball and pit alignment characteristic for packaging appears robust since internal vibrations add minimal noise to the link. In essence the 4.0 dB optical loss associated with packaged OPxC appears like a static attenuator of the optical signal. On a six-axis aligner the loss was measured to be 3.5dB per OPxC hop and hence the package contributes approximately 0.5 dB attenuation. According to the misalignment calculations in Figures 3 this implies package error  $<1\mu\text{m}$  for OPxC. Most of the OPxC loss arises from the excess loss associated with the fabrication of the reflecting pit and can be reduced. Our current results were obtained from the first fabrication iteration on this new technology and we expect to improve it in future iterations. Finally we observe broadband transmission for OPxC between 1500 and 1600 nm.



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